Navy Case No. 75881

COMPLEMENTARY VERTICAL BIPOLAR JUNCTION TRANSISTORS FABRICATED OF SILICON-ON-SAPPHIRE UTILIZING WIDE BASE PNP TRANSISTORS

BACKGROUND OF THE INVENTION

This invention relates generally to a method for making bipolar transistors. More particularly, the invention relates to a method of making complementary vertical bipolar junction transistors fabricated in silicon on a sapphire substrate.

Many semiconductor electronic devices are fabricated on a bulk, crystalline, silicon substrate. Yet, for a number of specific devices and applications, a better choice of substrate material is sapphire. In such cases, a thin layer of silicon is deposited on an insulating sapphire base. This combination has become known as silicon-on-sapphire, and is a specific example of what is known as silicon-on-insulator technology.

Bipolar junction transistors fabricated of silicon-on-sapphire technology have several important advantages when compared to transistors fabricated on bulk silicon. Total isolation between transistors is possible by removing any silicon surrounding the transistors down to the sapphire level. This produces an island that inhibits cross-talk between closely located devices and improves chip reliability when packing density is high.

It is known that bipolar transistors experience problems associated with parasitic capacitance. The severity of this capacitance increases as transistors are made smaller. Because of the insulating qualities of the sapphire substrate, relatively little capacitance between a transistor's collector and the sapphire will exist. In addition, all interconnecting lines can be

located on the sapphire substrate, thereby contributing little to parasitic capacitance. This allows high-frequency components to be located relatively near one another on the same chip, with the benefit of unwanted feedback being eliminated or substantially reduced. Thus the speed and reliability of transistors fabricated of silicon-on-sapphire is typically enhanced.

It is also known that silicon-on-sapphire devices are more radiation hardened than those fabricated on bulk silicon. Such radiation hardness permits devices to operate more effectively in environments containing high levels of ionizing radiation.

While the attributes of fabricating bipolar junction transistors of silicon-on-sapphire are well known, such fabrication has been accomplished with varying degrees of success. An early approach to fabricating this type of transistor based on silicon epitaxial growth on a sapphire substrate can be found in U.S. Pat. No. 4,050,965. This patent describes a process for fabricating bipolar junction transistors integrated with CMOS devices formed laterally on the same integrated circuit. Other early examples of methods for making bipolar transistors of silicon-on-sapphire can be found in U.S. Pat. No. 3,943,555 which discloses the use of ion implantation to produce a planar bipolar junction transistor that is isolated on a substrate. United States Pat. No. 3,974,560 discloses the use of ion implantation and diffusion to fabricate a lateral bipolar transistor.

More recent methods for fabricating a lateral bipolar junction transistor can be found in U.S. Pat. No. 5,298,786, which describes the use of polysilicon in the fabrication of a transistor having an edge-strapped base contact. United States Pat. No. 5, 198,375 discloses the use of a dielectric layer to form both vertical and lateral transistor devices. United States Pat. No. 5,374,567 describes a method of fabricating a low leakage current bipolar junction transistor on

silicon-on-sapphire for use in operational amplifiers utilizing all-implant technology, improved silicon conditioning and low temperature annealing. In U.S. Patent No. 5,714,793, an intricate process is used to fabricate true complementary vertical bipolar junction transistors of silicon-on-sapphire.

Most of the development of bipolar junction transistors of silicon-on-sapphire has been concentrated in the area of lateral bipolar junction transistors, epitaxial vertical bipolar junction transistors, and heteroepitaxy bipolar junction transistors. This work has been recorded respectively by P.K. Vasudev in his article in *IEEE Circuits and Devices* magazine titled: Recent Advances in Solid-Phase Epitaxial Recrystallization of SOS with Applications to CMOS and Bipolar Devices, of July 1987, pp. 17-19; by F.P. Heiman and P.H. Robinson in their article in *Solid State Electronics* titled: Silicon-on-Sapphire Epitaxial Bipolar Transistors of 1968, Volume 11, pp. 411-418; and by E.N. Cartagena, B.W. Offord and G. Garcia in their article in *Electronics Letters* titled: Bipolar Junction Transistors Fabricated in Silicon-on-Sapphire of 1992, Volume 28, pp. 983-985.

Traditional bipolar circuitry relies on high performance vertical devices for many of the circuit dynamic functions, while lateral devices provide the biasing and loading functions of the circuit. Experience has shown that lateral devices provide poor circuit element performance, such as low current gain, inadequate current carrying capability and low frequency response. In addition, lateral bipolar transistors occupy a relatively large area of a substrate and typically have high parasitic capacitance. In many applications, limitations of a circuit are determined by the poor performance of the lateral devices. As a consequence, vertical bipolar transistors are commonly chosen for use in high performance/high speed integrated circuits.

Complementary bipolar circuits with high performance vertical devices in the signal path offer enhanced capability of push-pull circuits for both analog and digital applications. Complementary bipolar circuits can also reduce power dissipation, increase switching speed and improve the flexibility of the overall circuit design.

Specific benefits gained by fabricating complementary bipolar circuits of silicon-on-sapphire technology include latch-up immunity, the ability to achieve high packing density, radiation hardness and the capability of operating circuits at a higher frequency response.

In a typical silicon-on-sapphire device, the thickness of the epitaxial layer of silicon on the sapphire base is between 0.5 and 5 micrometers (μm). The quality of this silicon epitaxial layer will play a direct role in the success of the silicon-on-sapphire device. Poor quality silicon will prevent the fabrication of a satisfactory bipolar junction transistor when diffusion of impurities into the silicon layer is required.

The silicon layer on a sapphire substrate will generally lack good crystal structure when compared to bulk silicon. In addition, a relatively higher density of defects in the epitaxial silicon will be found when compared to bulk silicon. A problem associated with the larger defect density is low minority carrier lifetime. Lifetimes that range from as low as 0.1 ns to 10 ns are typical for these epitaxial layers, compared to minority carrier lifetimes of 100 ns to 1 microsecond or more for bulk silicon. Since a bipolar junction transistor is a minority carrier device, efficient operation requires a relatively high minority carrier lifetime in the base region.

To improve the quality of a silicon epitaxial layer on a sapphire base, rescrystallization techniques have been used. One such process, known as the double solid phase epitaxy technique, has been described by P.K. Vasudev in his 1987 article in *IEEE Circuits and Devices*

noted above.

While rescrystallization techniques improve the quality of the silicon epitaxial layer, further improvements are required to make bipolar junction transistors more practical for many semiconductor circuit applications. Such practicality could be advanced by a process of fabricating complimentary vertical bipolar junction transistors having fewer steps than those required for true complementary vertical bipolar junction transistors.

SUMMARY OF THE INVENTION

The invention is a method for fabricating complementary vertical bipolar junction transistors of silicon-on-sapphire in fewer steps than required for true complimentary vertical bipolar junction transistors. Initially a thin layer of silicon is grown on a sapphire substrate. The silicon layer is improved using double solid phase epitaxy. The silicon is then patterned and implanted with P+-type and N+-type dopants. Subsequently a micrometer scale N-type layer is grown that acts as both the intrinsic base for an PNP transistor and as the collector for an NPN transistor. The intrinsic base for the NPN is then formed, followed by the emitter, collector and ohmic contact regions being selectively masked and implanted. Conductive metal is then formed between protecting oxide to complete the complementary vertical bipolar junction transistors.

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An object of the invention is to provide an improved method for fabricating bipolar junction transistors.

Another object of the invention is to provide an improved method for fabricating vertical bipolar junction transistors.

Yet another object of the invention is to provide an improved method for fabricating complementary vertical bipolar junction transistors.

Yet still another object of the invention is to provide a simplified method for fabricating complementary vertical bipolar junction transistors.

Still another object of the invention is to provide an improved method for fabricating complementary vertical bipolar junction transistors of silicon-on-sapphire.

Still a further object of the invention is to provide an improved method for fabricating complementary vertical bipolar junction transistors of silicon-on-sapphire utilizing wide base PNP transistors.

Other objects, advantages and new features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanied drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B show cross-sectional views of complementary vertical bipolar junction transistors as may be fabricated according to the invention.

FIGS. 2-41 show exemplary processing steps for fabricating complementary vertical bipolar junction transistors of silicon-on-sapphire according to the invention.

FIG. 42 illustrates a cross-sectional view the complementary vertical bipolar junction transistors according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGS. 1A and 1B, cross-sectional views of complementary vertical bipolar junction transistors 10 fabricated of silicon-on-sapphire according to the invention is shown. The elements of these transistors will be discussed first. Following this will be a discussion of the steps used to fabricate these transistors.

The complementary vertical bipolar junction transistors include PNP vertical transistor 12 and NPN vertical transistor 14 sharing a sapphire substrate 16. Base region 18 of PNP transistor 12 is formed of silicon of N-type conductivity. Region 18, also shown as "B", is of a wide base and is disposed to contact collector region 20. Collector region 20, also shown as "c", includes silicon with P+-type conductivity and is disposed in contact with sapphire substrate 16. Emitter region 22, shown also as "e", includes silicon with P+-type conductivity and is formed within base region 18 of PNP transistor 12. Also formed within base region 18 are ohmic contacts 23 ("b") that are used in conjunction with some conducting metal contacts "m".

NPN vertical bipolar junction transistor 14 includes collector region 24 ("c") of silicon with N-type conductivity. Collector region 24 is disposed in contact with sub-collector ("sc") region 26 which further lies in contact with substrate 16. Base region ("B") 28 of vertical bipolar transistor 14 is composed of silicon with P-type conductivity. Emitter region 30 ("e") is of silicon with N+-type conductivity and is formed within base region 28. Also formed within base region 28 are ohmic contacts "b" for use with some of the conducting metal contacts "m". As is shown in FIG. 1B, conducting metal surfaces ("m") are illustrated as well as are oxide layers "o".

Vertical bipolar PNP transistor 12 and vertical bipolar NPN transistor 14 are physically isolated from one another, to minimize cross-talk. This is accomplished by removing conducting silicon from region 32 between the two transistors. The only remaining material in contact with PNP transistor collector 20 and NPN transistor sub-collector region 26 is insulating sapphire substrate 16.

Referring now to FIGS. 2-27, an exemplary series of semiconductor processing steps according to the invention are shown. These steps may be used to fabricate the complementary

vertical bipolar transistors of silicon-on-sapphire according to the invention.

Referring to FIG. 2, a wafer 34 includes a layer 36 of silicon grown on a sapphire substrate 38 by any traditional method such as heteroepitaxy. This layer may be approximately 0.3 micrometers thick, for example, however other thicknesses may be used. The quality of the grown silicon is improved by a rescrystallization technique such as double solid phase epitaxy, described by P.K. Vasudev in his 1987 article in *IEEE Circuits and Devices* noted above and incorporated by reference herein.

Such recrystalization processing is illustrated in FIGS. 3-6, and begins with reference to FIG. 3 with the amorphization of silicon at silicon-sapphire interface region 40. The amorphization may be accomplished by using an implant of Si^{28} at an energy of 185 kilo-electron volts (KeV) and at a dose of 6×10^{14} ions/cm^2, for example.

Referring to FIG.4, the rescrystallization improvement process is shown furthered in which an anneal in an inert gas such as nitrogen (N_2) is used to recrystallize wafer 34 using non-amorphized upper region 36 as a seed.

The next step is illustrated in FIG. 5 wherein silicon at surface layer 42 is amorphized by using a shallow implant of Si^{28} at an energy level of 100 KeV and an implant dose of 10^{15} ions/cm^2 for example.

Referring to FIGS. 5 and 6, the recrystallization process is completed with a final anneal in an ambient gas such as N_2 that recrystallizes the silicon surface layer 42 using non-amorphized bottom layer 44 as a seed.

Following the annealing and prior to ion implantation, a thin oxide layer 46 illustrated in FIG.7 is grown uniformly across wafer 34. An oxide layer found suitable is approximately 0.025

micrometers thick, however other thicknesses may prove suitable as well.

In FIG. 8 an implantation is performed to form a P+ region in wafer 34 to begin the formation of collector region 20 of PNP transistor 12 illustrated in FIG. 1. Wafer 34 is coated with photoresist, and the photoresist is removed in the region where implantation is desired. The technique of depositing photoresist onto a wafer and selectively removing it in specific regions of the wafer creates a mask or pattern and is well-known to those of ordinary skill in the art of semiconductor processing.

Referring again to FIG. 8, photoresist 48 is used to mask region 50 of silicon layer 52. Masking prevents the implanted ions from penetrating into region 50. Where there is no photoresist masking, region 54 of silicon layer 52 is implanted with ions that penetrate the region. Implantation that may used to produce the desired P+ region is a boron implantation of BF_2 gas at 30 KeV with a dose of $1.5x10^{15}$ ions/cm^2 followed by a second dose of $1.5x10^{15}$ ions/cm^2 at 70 KeV, for example. After the implantation step illustrated in FIG.8, the photoresist layer 48 is removed by a conventional method such as by ashing, for example.

FIG. 9 illustrates a process used to create an N+ region in wafer 34 that is part of sub-collector region 26 of NPN vertical transistor 14 illustrated in FIG. 1. Photoresist layer 56 is produced by coating all of wafer 34 with photoresist and selectively removing the resist from certain regions of the wafer as is well-known to those knowledgeable in the art of semiconductor processing. Implantation to form the N+ region may utilize arsenic (As) ions for example at 80 KeV at a does of $3x10^{15}$ ions/cm^2. Photoresist layer 56 prevents the ions from penetrating into region 58. However the As ions readily penetrate into region 60 of wafer 34.

FIG. 10 illustrates the next step of the process. The oxide layer is first removed in region

62 above the P+ and N+ regions 64 and 66, respectively. Oxide removal can be accomplished by etching for example, or another technique well-known to those knowledgeable in the art of semiconductor processing. A silicon layer 68 is then epitaxially grown on wafer 34. For purposes of this invention, this layer is approximately 2.5 micrometers thick, however layers of other thicknesses may work as well. This layer is doped for N-type conductivity and may contain arsenic of approximately 10^{16} ions/cm^3 for example. Layer 68 acts as the intrinsic base for the PNP transistor and the collector for the NPN transistor.

FIG. 11 illustrates the next step in the wafer processing. A thin oxide layer 70 is grown on N-type layer 68 of wafer 34. Oxide layer 70 is thermally grown to 250 angstroms thick and is used as a masking layer.

After growth of the oxide layer, a photoresist mask or pattern 72 is placed on oxide layer 70 as illustrated in FIG. 12. The photoresist mask is used to define island regions. As illustrated in FIG. 13, oxide layer 70 is removed by etching in regions where the oxide layer is not protected by phototresist pattern 72. Such etching may be performed by using a buffered oxide etch for example or by any other technique known to those skilled in the art.

In FIG. 14, a subsequent etching takes place such as that which may be produced by a potassium hydroxide etching at an elevated temperature of approximately 100° C for example, to remove undesired silicon material. The removal of silicon is desired to define islands 74 and 76, and to remove any silicon in region 78 down to insulating sapphire layer 38. Photoresist pattern 72 is then removed by ashing, for example or any other suitable method, as shown in FIG. 15. Another etching step is shown in FIG. 16 and may be performed with a buffered oxide, for example or other sufficient technique. This etching step is required to remove the remaining

oxide 70 from wafer 34. Island 80 will eventually become a PNP vertical transistor, while island 82 will eventually become a NPN vertical transistor.

Wafer 34 then goes through an oxide growth stage as illustrated in FIGS. 17-19. At the beginning of this stage, as illustrated in FIG. 17, wafer 34 is placed in a furnace at approximately 875° C for example. Initially, the ambient gas in the furnace may be N_2 for example. As shown in FIG. 18 once wafer 34 is completely contained inside the furnace, hydrogen and oxygen may be added to the ambient nitrogen to provide an oxidizing atmosphere for oxide growth of approximately 250 angstroms, for example. After the growth of oxide layer 84 as illustrated in FIG.19, wafer 34 is slowly pulled out of the furnace into a controlled environment such as pure nitrogen gas.

Referring to FIG. 20, after the oxide growth, wafer 34 is patterned with photoresist layer 86 to produce the intrinsic base region for the NPN transistor. Open patterned area 88 defines a region for an active P-doped base area for the NPN vertical transistor to be fabricated. As illustrated in FIG. 20, wafer 34 is implanted with a P-type dopant such as boron, applied at the appropriate dose and energy level to yield desired electrical results. In general, the desired electrical results comprise preselected ranges of values for the breakdown voltage, current gain, leakage current and frequency response which enhance the operation of the complementary vertical bipolar transistors fabricated according to the invention.

Following the implantation step illustrated in FIG. 20, photoresist layer 86 is removed by ashing for example. As illustrated in FIG. 21, placing wafer 34 inside an oven anneals the damage done during implantation and moves inactive implanted species into the crystal lattice of the silicon, making it electrically active. The ambient gas used may be nitrogen and the furnace

temperature may be approximately 900-950° C for example.

In the next step of processing, both the extrinsic base region of the NPN transistor and the emitter region of the PNP transistor are fabricated by ion implantation.

As illustrated in FIG. 22, photoresist layers 90, 92, 94, 96 and 98 form a pattern on oxide layer 84. Open patterned area 102 defines the emitter region for the PNP transistor. Open patterned areas 104 and 106 define the extrinsic base region for the NPN transistor. As illustrated in FIG. 23, wafer 34 is implanted with boron ions at an appropriate dose and a high energy level to yield desired electrical results, for example, dose of 10^{17} ions/cm^2 at 650 KeV. The high energy ions permit penetration of the boron into open areas 108, 84 and 112 illustrated in FIG. 23 as well as in the open patterned areas 114 and 116. The opened pattern areas 114 and 116 define regions to which metal will make eventual contact to form an ohmic contact to the intrinsic base region 118 illustrated in FIG. 22 of the vertical NPN transistor. Penetration of the boron into areas 108 and 112 illustrated in FIG. 23 produces collector plugs 120 and 122, shown in FIG. 24. Collector plugs 120 and 122 are incorporated into the structure of the vertical PNP transistor fabricated according to the invention to help reduce series collector resistance. Following the implantation step illustrated in FIG. 23, photoresist layers 90, 92, 94, 96 and 98 illustrated in FIG. 22 are removed by ashing or by plasma etching for example as illustrated in FIG. 24.

FIG. 25 illustrates the next step in the processing of the vertical bipolar junction transistors. In this step the extrinsic base contacts for the PNP transistor and the emitter for the NPN transistor are fabricated. Wafer 34 is patterned with photoresist 124 to include open areas 126, 128, 130, 132 and 134. Implantation of arsenic (As) as shown, may be used to create N+

areas in wafer 34. The dosage and energy of the implantation are relatively high and are selected to produce the desired electrical results, for example, a dose of As ions of $5x10^{21}$ ions/cm^2 at 150 KeV. The open pattern areas 126 and 128 define regions to which metal will make eventual contact to form an extrinsic base to the PNP transistor. Open pattern region 132 defines the region that is to form the emitter region of the NPN transistor. Penetration of the As into areas 130 and 134 produces collector plugs in regions 136 and 138 shown in FIG. 26. Collector plug regions 136 and 138 are incorporated into the sub-collector region of the vertical NPN transistor fabricated according to the invention to help reduce series collector resistance.

Following implantation the photoresist is removed by ashing or other typical means as illustrated in FIG. 26. The impurities that are implanted into wafer 34 are activated by a thermal method as illustrated in FIG. 27. This method comprises inserting the wafer in a furnace of nitrogen atmosphere. The temperature is then ramped up to a predetermined value, generally in the range of 850C to 900 C. This thermal temperature serves to both anneal the damage done to the crystalline lattice by ion implantation as well as to move the substitutional impurities into the crystalline lattice to make them electrically active.

Following the thermal activation step illustrated in FIG. 27, additional steps of metal deposition, etching and annealing are performed as illustrated in FIGS. 28-34. As illustrated in FIG. 28, a layer of additional oxide 140 is deposited. This layer may be 0.5 micrometers thick for example. As shown in Fig. 29 wafer 34 is annealed in a controlled ambient such as nitrogen (N_2) at a temperature of 850 C for one hour. FIG. 30 shows photoresist mask 142 in place to define areas 144 of wafer 34 to which conducting metal will eventually be deposited. Photoresist mask 142 is known as the contact level mask.

As can be seen in FIGS. 31 and 32, previously deposited oxide layer 84 of FIG.19 and oxide layer 140 of FIG. 28 have been etched by way of a buffered oxide etch, for example, to expose areas 146, 148, 150 and 152. In FIG. 32 photoresist contact mask 142, shown in FIG. 31, is removed by ashing, for example. As illustrated in FIG. 33 conducting metal 154 is deposited on wafer 34. The conducting metal may be 1 micrometer thick, for example, and include of aluminum containing 1% silicon, for example. Of course, other suitable conductors may be used as well.

In FIG. 34, photoresist mask 156 is deposited in a pattern to define the areas where conducting metal is to remain to provide ohmic contacts for the complementary bipolar junction transistors fabricated according to the invention. In FIG. 35 the conducting metal is etched, as by plasma etching or other suitable method, for example. Following the etching of the conducting metal, wafer 34 includes photoresist pattern 156, conducting metal pattern 158 and oxide pattern 160 as illustrated in FIG. 35. The next step removes photoresist mask 156 from wafer 34 as illustrated in FIG. 36. Removal of mask 154 may be accomplished by ashing or plasma etching or other sufficient method for example. In FIG. 37 wafer 34 undergoes an annealing step at an exemplary temperature of 400 C. This step sinters the metal aluminum composition in the silicon to provide good ohmic contact to the complementary bipolar junction transistors.

In FIG. 38 an additional oxide layer 162 is deposited. The oxide layer may have a thickness of 0.5 micrometers for example. In FIG. 39 oxide photoresist pattern 164 is deposited over oxide layer 162 to define regions on wafer 34 where the oxide will remain. FIG. 40 illustrates the etching of the oxide through photoresist pattern 164, and FIG. 41 shows the removal of the photoresist by ashing or other suitable method for example.

FIG. 42 shows complementary vertical bipolar junction transistors 10 fabricated according to the steps disclosed in FIGS. 2-41. The vertical PNP and NPN transistors are illustrated in cross section. and the letters "sc", "c", "b" and "e" denote the sub-collector, collector, base and emitter, respectively. Further, the letters "m" and "o" indicate regions containing conducting metal and oxide, respectively.

Obviously, many modifications and variations of the invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may be practiced other that as has been specifically described.